REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 2 November 2004. Responsive to the objections and rejections made by the Examiner in the Official Action, Claims 1-10 have been amended and are now clearer in their respective recitations. Claims 1-10 will be pending in this Application upon entry of the Amendment filed herewith.

In the Official Action, the Examiner objected to Claims 3 and 4 because of informalities. Accordingly, Claims 2-4 (Claim 2 having been discovered to contain the same error) have been amended to replace the word "Clam" with the correct word "Claim".

In the Official Action, the Examiner rejected Claims 1-3 and 5-7 under 35 U.S.C. § 102(b) as being anticipated by Fujii, et al. (U.S. Patent 5,898,695; hereinafter Fujii). In setting forth this rejection, the Examiner equated the packet landing buffer 71 of Fujii with the claimed ring buffer and further equated the claimed error resilience module with contents of program memory 205 recited by Fujii.

The Examiner further rejected Claims 4 and 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Fujii as applied to Claims 1 and 6, and further in view of Kadono (U.S. Patent 6,757,332). The Examiner relied on the teachings of Kadono to show an MPEG-4 compliant decoder in that Fujii teaches only an MPEG decoder. The Examiner concluded that it would have been obvious to one

of ordinary skill in the art to incorporate the MPEG-4 compliant decoder of Kadono into the video bitstream decoder of Fujii for the purpose of decoding any video encoded bitstreams.

Applicant's data management systems and methods utilize a ring buffer to store a video bitstream during an error resilient decoding process performed thereon. The data may thereby be read from the video bitstream multiple times, from multiple locations and in multiple directions. Thus, the ring buffer includes, as recited in amended Claim 1, "a predetermined number of memory locations, the video bitstream being stored in either sequentially increasing or sequentially decreasing addresses as received ..., data stored in the ring buffer being accessible by both sequentially increasing memory addresses and sequentially decreasing memory addresses". The ring buffer may then be coupled to an error resilience module which is "operable to select either an error correction procedure from a plurality of error correction procedures or to select no error correction procedure, the selection responsive to analysis of the video bitstream in both the forward direction and a reverse direction as accessed via the ring buffer". The utility of the inventive configuration is clearly set forth in the Specification of the subject Patent Application.

To maximize the versatility of the invention of the subject Patent Application, the ring buffer may be used in conjunction with a means for storing data logging information. Data logging information is stored in the ring buffer

"aligned in memory with the corresponding video bitstream data" such that "both a portion of the video bitstream data from the ring buffer and a corresponding portion of the data logging information from the ring buffer [is automatically retrieved] responsive to a request for retrieving the portion of the video bitstream data from the ring buffer" as recited in amended Claims 5 and 6. Thereby, data logging information, including error logging information such as error flags, may be stored in the ring buffer as it is generated by an error inspecting means. Thus, the data logging means may provide information to subsequent error correcting means, where the error correcting means is selected in accordance with analysis performed on the video data held in the ring buffer.

The full combination of these and other features now more clearly recited by Applicant's pending claims is nowhere disclosed by the cited Fujii reference. As the Examiner recognized, Fujii does disclose a data buffer (packet landing buffer 71) which may be addressed in circular fashion as shown in Fig. 6 of the Fujii reference. However, as clearly pointed out in column 6, lines 14-17, "the packet landing buffer 71 is a first-in-first-out (FIFO). Only one packet is written in each line in the landing order, and read in the same order" (emphasis added). Thus, Fujii teaches away from Applicant's claimed ring buffer which allows data to be accessed "by both sequentially increasing memory addresses and sequentially decreasing memory addresses".

Arguendo, even if the ring buffer of Fujii were allowed to be operable in multiple directions, it is not used in an error resilient decoding system as defined by the now pending claims of the subject Patent Application. In setting forth the rejections, the Examiner referred to Fig. 17 of Fujii in showing equivalence of RAM 203 to the claimed ring buffer and equivalence of error correction demodulator 201 with the claimed means for inspecting the video bitstream for error. However, error correction demodulator 201 actually corrects errors and sends an error corrected encoding stream, a sync signal and an error flag to the channel demultiplexer (column 11, lines 61-67). Thus, data stored in the landing buffer of Fujii can only be that of corrected data and not capable of "storing the video bitstream in a ring buffer subsequent to the video bitstream being inspected for error and prior to correction thereof" as is now recited by the pending claims. Moreover, the error flag adder 217, the element cited by the Examiner as fulfilling the limitation of the claimed means for storing data logging information, provides error indication to data that has already been corrected by error correction demodulator 201. Thus, Fujii does not show, or even suggest, the combination of a "storing the video bitstream in a ring buffer subsequent to the video bitstream being inspected for error and prior to correction thereof" and "means for storing data logging information corresponding to the video bitstream data in the ring buffer". As is clear from the Specification of the subject Patent Application, the unique combination of elements and method steps provides great flexibility in

selectively deciding an appropriate error correction procedure based on an analysis performed on data in the ring buffer; the data logging information providing ancillary information such as error flags to provide even further flexibility.

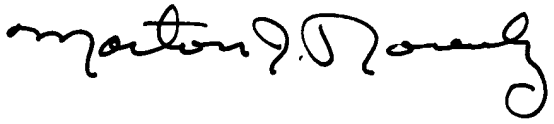
Given such contrary teachings of the primarily cited Fujii reference, the disclosures of the secondarily cited Kadono reference are found to be quite ineffectual to the present patentability analysis. While Kadono does show the use of a MPEG-4 decoder and the related use of video object plane (VOP) data, the reference does not show, or even suggest, the claimed ring buffer elements and associated method steps now claimed.

It is respectfully submitted, therefore, that the Fujii and Kadono references, even when considered together, fail to disclose the unique combinations of elements and related method steps now more clearly recited by Applicant's pending claims for the purposes and objectives disclosed in the subject Patent Application.

The remaining Patent cited by the Examiner but not used in the rejections has been reviewed, but is believed to be further remote from the subject Patent Application than the references used by the Examiner when patentable considerations are taken into account.

In view of the foregoing amendments and remarks, Applicant believes that the subject Patent Application is in condition for allowance and such action is respectfully requested.

Respectfully submitted,
For: ROSENBERG, KLEIN & LEE



Morton J. Rosenberg
Registration #26,049

Dated: 2/1/05

Suite 101
3458 Ellicott Center Drive
Ellicott City, MD 21043
(410) 465-6678